AMENDMENTS TO THE CLAIMS:

The present Amendment has been prepared in accordance with a revised format established by the U.S. Patent and Trademark Office, as permitted in the Pre-OG Notice entitled "Amendments in a Revised Format Now Permitted."

Please amend Claims 1, 18, and 49-51, and add new Claims 52-54, as follows. In accordance with the revised amendment format, all claims are presented below.

1. (Currently Amended) A driving apparatus comprising:

~~A~~ a matrix substrate having plural pairs of switching elements and picture elements provided in a matrix corresponding to intersecting points of scanning lines and signal lines; ~~, plural picture element electrodes connected to the switching elements, and horizontal circuits and vertical circuits for inputting the signals to the switching elements, the matrix substrate comprising:~~

an input terminal for ~~inputting~~ receiving a sequence of digital video data in a serial fashion;

a vertical scanning circuit for outputting a scanning signal to the scanning lines;

a sequencing circuit for changing an initial sequencing order of the digital video data ~~inputted through~~ received at said input terminal into a different sequencing order, and for serially outputting the digital video data in the different sequencing order;

a horizontal scanning circuit for controlling a sampling of the digital video data in the ~~initial~~ different sequencing order;

a latch circuit for memorizing the digital video data ~~synchronously~~ in its different sequencing order in synchronism with an output from the horizontal scanning circuit;

a D/A converter for converting an output from the latch circuit into analog signals;

plural signal transfer switches provided between the D/A converter and the signal lines;

a selection circuit for selecting at least one of the signal transfer switches so as to output said analog signals to the matrix substrate in the same order as the different sequencing order of the digital video data;

polarity inversion circuitry which ~~inputs signal-polarity inverting signals together with the picture data, and which inverts the polarity of the~~ controls said D/A converter to alternately invert the analog signal from the D/A converter; and

a buffer disposed between said D/A converter and said selection circuit, which stores the analog signal ~~of inverted polarity~~ from the D/A converter, and outputs said stored signal to said plural signal transfer switches,

wherein a number M of said D/A converters is less than a number N of said switching elements arranged in a horizontal direction, and analog signals are sequentially inputted from particular ones of said M D/A converters to N/M plural switching elements arranged in a horizontal direction, via a number M of said buffers.

2. (Original) The matrix substrate according to claim 1, wherein the analog signals are applied to the signal lines through the transfer switches in every output of the selection circuit.

3. (Cancelled)

4. (Original) The matrix substrate according to claim 1, wherein the selection circuit is constituted of a shift register.

5. (Previously Presented) The matrix substrate according to claim 1, wherein the switching element is a CMOS transistor.

6. (Cancelled)

7. (Original) The matrix substrate according to claim 1, wherein the D/A converter is capable of inputting one bit more than the bit number of the picture data bits, and the signal-polarity inverting signal is inputted to the most significant bit of the D/A converter.

8. (Original) The matrix substrate according to claim 1, wherein the matrix substrate comprises a changeover switch for selecting one of at least two groups of the signal transfer switches to be inputted from the D/A converter.

9. (Original) The matrix substrate according to claim 8, wherein the picture data is supplied in divisions, and sampling is conducted by the horizontal scanning circuit.

10. (Original) The matrix substrate according to claim 9, wherein the matrix substrate comprises a means for changeover of the divided picture data.

11. (Original) The matrix substrate according to claim 1, wherein the matrix substrate has an elevation circuit for boosting the output of the D/A booster.

12. (Original) The matrix substrate according to claim 11, wherein the booster circuit comprises a clamp type amplifier.

13. (Original) The matrix substrate according to claim 1, wherein the D/A converter provides analog signals by selecting one point of a resistance element connected in series by decoding digital signals of more significant bit and less significant bit.

14. (Original) The matrix substrate according to claim 13, wherein said resistance element for a resistance division is comprised of a diffusion layer in a semiconductor substrate, and an impurity concentration of a diffusion layer comprising the resistance element for the more significant bit is higher than that comprising the resistance element for the less significant bit.

15. (Original) The matrix substrate according to claim 1, wherein the D/A converter comprises at least two analog buffer circuits and a circuit for selecting one of the two buffer circuits.

16. (Original) The matrix substrate according to claim 15, wherein the two buffer circuits are employed respectively for positive polarity and for negative polarity.

17. (Original) The matrix substrate according to claim 1, wherein the picture element electrode is polished by chemical mechanical polishing.

18. (Currently Amended) A liquid crystal device comprising a matrix substrate having plural pairs of switching elements and picture elements provided in matrix corresponding to intersecting points of scanning lines and signal lines, ~~plural picture element electrodes connected to the switching elements,~~ and horizontal selecting circuits and vertical scanning circuits for inputting ~~the~~ signals to the switching elements; a counter substrate ~~opposing~~ opposed to the matrix substrate; and a liquid crystal material placed between the matrix substrate and the counter substrate, the matrix substrate comprising:

an input terminal for ~~inputting~~ receiving a sequence of digital video data in a serial fashion;

a sequencing circuit for changing an initial sequencing order of the digital video data ~~inputted through~~ received at said input terminal into a different sequencing order, and for serially outputting the digital video data in the different sequencing order;

a horizontal scanning circuit for controlling a sampling of the digital video data in the ~~initial~~ different sequencing order;

a latch circuit for memorizing the digital video data ~~synchronously~~ in its different sequencing order in synchronism with an output from the horizontal scanning circuit;

a D/A converter for converting the output from the latch circuit into analog signals;

plural signal transfer switches provided between D/A converter and the signal lines;

a buffer disposed between said D/A converter and said plural signal transfer switches, which stores the analog signal ~~of inverted polarity~~ from the D/A converter, and outputs said stored signal to said plural signal transfer switches;

a selection circuit for selecting at least one of the signal transfer switches so as to output said analog signals to the matrix substrate in the same order as the different sequencing order of the digital video data; and

means for ~~inputting signal-polarity inverting signals together with the picture data, and for inverting~~ controlling said D/A converter to alternately invert the polarity of the analog output of the D/A converter,

wherein a number M of said D/A converters is less than a number N of said switching elements arranged in a horizontal direction, and analog signals are sequentially inputted from particular ones of said M D/A converters to N/M plural switching elements arranged in a horizontal direction via a number M of said buffers.

19. (Original) The liquid crystal device according to claim 18, wherein the analog signals are applied to the signal lines through the transfer switches in every output of the selection circuit.

20. (Cancelled)

21. (Original) The liquid crystal device according to claim 18, wherein the selection circuit is constituted of a shift register.

22. (Previously Presented) The liquid crystal device according to claim 18, wherein the switching element is a CMOS transistor.

23. (Cancelled)

24. (Original) The liquid crystal device according to claim 18, wherein the D/A converter is capable of inputting one bit more than the bit number of the picture data bits, and the signal-polarity inverting signal is inputted to the most significant bit of the D/A converter.

25. (Original) The liquid crystal device according to claim 18, wherein the matrix substrate comprises a changeover switch for selecting one of at least two groups of the signal transfer switches to be inputted from the D/A converter.

26. (Original) The liquid crystal device according to claim 25, wherein the picture data is supplied in divisions, and sampling is conducted by the horizontal scanning circuit.

27. (Original) The liquid crystal device according to claim 26, wherein the matrix substrate comprises a means for changeover of the divided picture data.

28. (Original) The liquid crystal device according to claim 18, wherein the matrix substrate has an booster circuit for boosting the output of the D/A converter.

29. (Original) The liquid crystal device according to claim 28, wherein the booster circuit comprises a clamp type amplifier.

30. (Original) The liquid crystal device according to claim 18, wherein the D/A converter provides analog signals by selecting one point of a resistance element connected in series by decoding digital signals of more significant bit and less significant bit.

31. (Original) The liquid crystal device according to claim 30, wherein said resistance element for a resistance division is comprised of a diffusion layer in a semiconductor substrate, and an impurity concentration of the diffusion layer comprising the resistance element for the more significant bit is higher than that comprising the resistance element for the less significant bit.

32. (Original) The liquid crystal device according to claim 18, wherein the D/A converter comprises at least two analog buffer circuits and a circuit for selecting one of the two buffer circuits.

33. (Original) The liquid crystal device according to claim 32, wherein the two buffer circuits are employed respectively for positive polarity and for negative polarity.

34. (Original) The liquid crystal device according to claim 18, wherein the picture element electrode is polished by chemical mechanical polishing.

35. (Original) A display apparatus, comprising a liquid crystal device set forth in claim 18.

36. (Original) The display apparatus according to claim 35, wherein the display apparatus comprises a reflection type liquid crystal panel as the liquid crystal device, and displays a picture image by introducing light emitted from a light source to the liquid crystal panel, and projecting reflected light through an optical system onto a screen.

37. (Original) The display apparatus according to claim 36, wherein the display apparatus employs a liquid crystal panel comprising a picture element unit array and a microlens array: the picture unit array having picture element units arranged two-dimensionally at a prescribed pitch on a substrate, the picture element unit having three

color picture elements, and a combination of a first and second color picture elements being arranged in a first direction and another combination of the first and a third color picture elements being arranged in a second direction with the first color element common to the both combinations; and the microlens array being arranged two-dimensionally above the picture element unit array at the pitch corresponding to the pitches of two color picture element combinations arranged in the first and second direction on the substrate.

38. (Previously Presented) The matrix substrate according to Claim 1, further comprising:

a buffer connected to an output of the D/A converter, which stores the analog signal of inverted polarity from the D/A converter.

39-48 (Cancelled)

49. (Currently Amended) A horizontal selecting circuit comprising:

an input terminal for ~~inputting~~ receiving a sequence of digital video data in a serial fashion;

a sequencing circuit for changing an initial sequencing order of the digital video data ~~inputted through~~ received at said input terminal into a different sequencing order, and for serially outputting the digital video data in the different sequencing order;

a horizontal scanning circuit for controlling a sampling of the digital video data in the ~~initial~~ different sequencing order;

a latch circuit for latching the ~~sequenced~~ digital video data ~~synchronously~~ in its different sequencing order in synchronism with an output from the horizontal scanning circuit;

a D/A converter for converting the digital video data output from the latch circuit into analog signals;

plural signal transfer switches provided between the D/A converter and plural signal lines;

a transfer switch selection circuit for selecting at least one of said ~~plurality of~~ plural signal transfer switches so as to output ~~the~~ said analog ~~signal~~ signals to the plural signal lines in the same order as the different sequencing order of the digital video data.

50. (Currently Amended) The horizontal selecting circuit according to claim 49, wherein said horizontal scanning circuit has a shift register.

51. (Currently Amended) The horizontal selecting circuit according to claim 49, wherein said signal transfer switch has a CMOS transistor.

52. (New) A video horizontal selecting circuit comprising:

an input terminal for receiving a sequence of digital video data in a serial fashion;

a sequencing circuit for changing the received sequencing order of the digital video data, such that data separated by N positions (N is an integer ≥ 2) become

adjacent, and for outputting the sequencing order-changed digital video data in a serial fashion;

a horizontal scanning circuit for controlling a sampling of the sequencing order-changed digital video data;

a latch circuit for latching the sequencing order-changed digital video data in synchronization with an output from the horizontal scanning circuit;

a D/A converter for converting the digital video data from the latch circuit into an analog signal; and

a transfer switch selecting circuit for selecting at least one signal transfer switch provided with a CMOS transistor to sequentially output the analog signal for digital video data separated by N positions in the sequencing order-changed digital video data.

53. (New) A drive circuit provided with a horizontal selecting circuit and a vertical selecting circuit, wherein said horizontal selecting circuit comprises:

an input terminal for receiving a sequence of digital video data in a serial fashion;

a sequencing circuit for changing the received sequencing order of the digital video data, such that data separated by N positions (N is an integer ≥ 2) become adjacent, and for outputting the sequencing order-changed digital video data in a serial fashion;

a horizontal scanning circuit for controlling a sampling of the sequencing order-changed digital video data;

a latch circuit for latching the sequencing order-changed digital video data in synchronization with an output from the horizontal scanning circuit;

a D/A converter for converting the digital video data from the latch circuit with an analog signal; and

a transfer switch selecting at least one signal transfer switch provided with a CMOS transistor to sequentially output the analog signal for digital video data separated by N positions in the sequencing order-changed digital video data.

54. (New) A display apparatus provided with a display panel having scanning lines and signal lines, a vertical scanning circuit arranged to be connected to the scanning lines and, a horizontal selecting circuit arranged to be connected to the signal lines, wherein said horizontal selecting circuit comprises:

an input terminal for receiving a sequence of digital video data in a serial fashion;

a sequencing circuit for changing the received sequencing order of the digital video data, such that data separated by N positions (N is an integer ≥ 2) become adjacent, and for outputting the sequence order-changed digital video in a serial fashion;

a horizontal scanning circuit for controlling a sampling of the sequencing order-changed digital video data;

a latch circuit for latching the sequencing order-changed digital video data in synchronization with an output from the horizontal scanning circuit;

a D/A converter for converting the digital video data from the latch circuit with an analog signal; and

a transfer switch selecting at least one signal transfer switch provided with a CMOS transistor to sequentially output the analog signal for digital video data separated by N positions in the sequencing order-changed digital video data.